POSTER

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An Architecture for Resilient Federated Learning Through Parallel Recognition

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ABSTRACT

In federated learning, non-independent and identically distributed (non-IID) local datasets lead to accuracy loss compared to homogeneous distribution of datasets. In this paper, we propose an architecture for improving accuracy and offering resilience through federation utilizing non-IID datasets. The proposed architecture performs parallel recognition employing triplication of AI processors with different intelligence. Experimental results demonstrate that the proposed architecture improves accuracy by 2.3% compared to accuracy of a single AI processor on average and guarantees resilience.

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1 INTRODUCTION

Federated learning allows collaboration of multiple intelligent edge devices without revealing private data [4]. The participating devices compute independently with local datasets and processed parameters are sent to central server. Previous works have demonstrated that non-independent and identically distributed (non-IID) local datasets cause reduced accuracy compared to homogeneous distribution of datasets [1]. However, imbalanced data distribution is required in many cases considering the various target environments of edge devices which have different power and area limitation or communication capability.

Recent works introduce solutions to address the accuracy loss and increase communication efficiency for non-IID federated learning. The work in [3] introduced central server that rates the local devices' performance utilizing reinforcement learning. To achieve optimized performance, they update the devices' weights repeatedly. Another work in [5] divides the local devices into different groups according to the distribution of datasets and set weight parameters based on the cosine distance. Such works provide efficient methods to improve accuracy but require additional steps and frequent communication between the central server and the local devices. Furthermore, the limited-resources issues which cause unstable communication and unreliable computation output still remain.

In this paper, we propose an architecture to improve accuracy with non-IID datasets and offer resilient federated learning. The triplication of AI processors with different intelligence; trained by different types or imbalanced amounts of learning datasets; collaborate with each other and enhance accuracy through parallel recognition. In addition, by sharing part of local learning datasets, the proposed architecture realizes indirect federation and becomes resilient. Experiments employing MNIST datasets demonstrate that the proposed architecture improves accuracy from 2.3% on average compared to the average accuracy of a single AI processor. Moreover, a FPGA implementation of the proposed architecture shows that the AI processors and the arbiter guarantees resilience and reliability with low-power consumption.

The main contributions of this paper are listed as follows:

- Through parallel recognition and federation of the AI processors, the proposed architecture achieves improvement of accuracy.
- Considering diverse target environments, the proposed architecture provides resilience with minimized participating devices by sharing learning datasets.
- For learning and parallel recognition process, the proposed architecture adopts lightweight algorithm resulting low-power consumption.

2 PROPOSED ARCHITECTURE

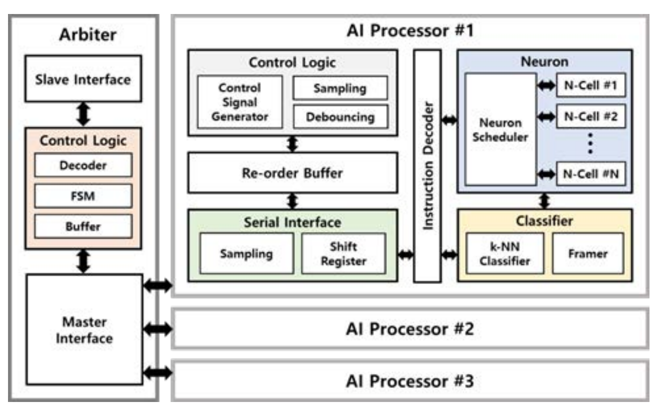

Figure 1: The overview of an architecture for resilient federated learning including triplication of AI processors and an arbiter

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The proposed architecture comprises three parallelized AI processors and an arbiter. We focus on improving accuracy with the AI processors which have different size and distribution of learning datasets. First, the AI processors send the parallel recognition outputs simultaneously to the arbiter. Second, in case of the recognition results from the majority of AI processors are identical, the result is adopted as a final recognition output. However, if three of the AI processors send different responses to each other, the final recognition output is determined by the most accurate AI processor. The accuracy of the AI processor is decided by accumulated recognition results in each process and only one AI processor obtains a weight parameter. As a result, the accuracy increases compared to the accuracy of a single AI processor through the cooperation of three AI processors.

Moreover, for each pair of AI processors (1 and 2, 2 and 3, and 1 and 3), the AI processors share part of learning datasets with each other. Consequently, if one of the AI processors malfunctions due to the insufficient learning datasets or communication error, the proposed architecture covers the fault result and provides resilience.

AI processor The AI processor is based on k-Nearest Neighbor (k-NN) algorithm and calculates the distance between learning datasets and recognition data with parallelized neuron cells. By applying the lightweight algorithm and Manhattan distance, the power consumption of the AI processor is reduced as multiplication units become unnecessary. As depicted in Figure 1, the re-order buffer sorts and reorders inputs received from the serial interface module. And the control logic determines read/write sampling timing to access neuron cells and generates memory operation signal to store the datasets. Then, the classifier assorts recognition datasets based on k-NN algorithm and performs parallel recognition. The recognition results from the AI processors are sent to the arbiter through the serial interface at the same time.

Arbiter The arbiter manages the AI processors and prevents data collision by scheduling the access timing. The arbiter receives selection signal of the AI processor from external system and activates the selected AI processors to learning/recognition mode. The arbiter aggregates recognition outputs from the AI processors and determines final recognition output.

3 EVALUATION

The accuracy of the proposed architecture was evaluated by ASimOV simulator [2]. For learning and recognition process, non-IID datasets, MNIST handwritten digit classification datasets are utilized as an input. Each of the AI processors includes 8192, 4096, and 2048 neuron memory cells. The AI processors in pairs 1 and 2, 2 and 3, and 1 and 3 share 516 randomly selected learning datasets with each other. As shown in Figure 2, the proposed architecture improves accuracy through federation by 2.3% on average, compared to the average accuracy of each AI processor. The improved accuracy is 0.48% above the highest accuracy of a single AI processor.

Furthermore, to evaluate the resilience, the AI processors and the arbiter are implemented on FPGA. The implementation of triplication architecture and overlapping part of the distributed learning datasets enables covering fault result on any one of the three AI processors and achieving resilience as shown in Figure 3.

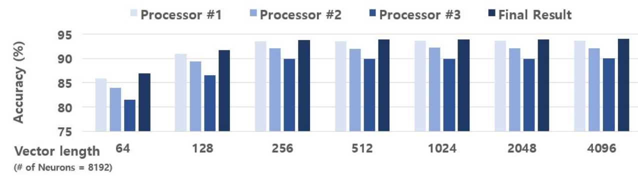

Figure 2: Comparison of the accuracy between single AI processor and the proposed architecture

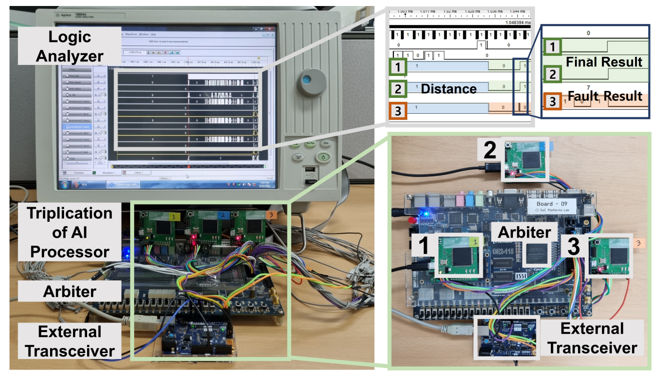

Figure 3: Experimental environments and recognition results from the logic analyzer

4 CONCLUSION

In this paper, an architecture to improve accuracy and provide resilient federated learning with triplication of parallelized AI processors is proposed. The parallelized AI processors collaborate with each other in order to increase accuracy utilizing non-IID datasets. The experimental result demonstrates that the proposed architecture not only enhances accuracy but provides resilience.

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